A marked-up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 CFR § 1.121(c)(1)(ii). Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

CLAIMS

1. (Amended) A method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle;

filling the first and second isolation trench portions with dielectric material; and

wherein the forming of the first isolation trench portion comprises forming the first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

2. The method of claim 1, wherein forming a second isolation trench portion includes forming the second angle to be between eighty and ninety degrees.

A1 Cont. 3. The method of claim 1, wherein forming a first isolation trench portion includes forming the first angle to be in a range of from about thirty degrees to about seventy degrees and forming a second isolation trench portion includes forming the second angle to be more than eighty degrees.

4. (Amended) The method of claim 1, wherein the semiconductor comprises silicon.

5. The method of claim 1, wherein forming a first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

6. The method of claim 5, wherein etching and depositing comprises:

providing a mixture of gasses chosen from a group consisting of CF_4, CHF_3, CH_2F_2 and C_2F_8; and

supplying radio frequency excitation to the mixture.

7. The method of claim 5, wherein etching and depositing comprises:

providing fluorocarbon gases; and

supplying radio frequency excitation to the mixture.

8. The method of claim 1, wherein forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

9. The method of claim 1, wherein forming the first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67;

depositing a polymer on the sidewalls during plasma etching;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing depositing polymer on the sidewalls; and

stopping etching and depositing when the predetermined interval ends.

10. Please cancel.

11. The method of claim 1, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

12. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

13. A method of forming an isolation trench in a surface of a silicon wafer comprising:

forming a mask on the surface, the mask including an opening and sidewalls; and

etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67 to form a first isolation trench portion, wherein the etching forms the opening and sidewalls in the mask.

14. The method of claim 13, wherein etching the silicon surface includes forming a first isolation trench portion having a first sidewall that intersects the silicon surface at an angle in a range of from about thirty degrees to about seventy degrees.

15. The method of claim 14, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

16. The method of claim 13, further comprising forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

17. The method of claim 16, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

18. The method of claim 17, further comprising:

filling the first and second isolation trench portions with dielectric material; and

planarizing the dielectric material filling the first and second isolation trench portions.

19. The method of claim 13, wherein forming a mask comprises:

forming a silicon nitride layer on the semiconductor surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

20. The method of claim 19, wherein etching the surface comprises:

plasma etching through the silicon nitride layer;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

21. The method of claim 19, further comprising forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

22. A method of forming an isolation trench-isolated transistor comprising:

forming first and second isolation trenches disposed to a respective side of a portion of silicon, forming the first and second isolation trenches comprising:

forming a mask on the surface, the mask including first and second openings corresponding to the first and second isolation trenches;

forming a first isolation trench portion in each of the first and second openings, each first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and

forming a second isolation trench portion within and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle; the method further comprising:

filling the first and second isolation trench portions with dielectric material;

forming a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions extending between the first and second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

23. The method of claim 22, wherein forming a first isolation trench portion comprises etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

24. The method of claim 22, wherein forming a mask comprises:

forming a silicon nitride layer on the semiconductor surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

25. The method of claim 22, wherein forming a first isolation trench portion comprises:

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined interval.

26. The method of claim 25, wherein plasma etching comprises etching using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

27. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the semiconductor at an angle in a range of from about thirty degrees to about seventy degrees.

28. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

29. The method of claim 27, wherein forming a second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface.

30. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

31. The method of claim 30, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

32. The method of claim 22, wherein the gate comprises polysilicon.

Please add the following new claims:

New Claims

62. (New) The method of claim 22 wherein the source region is disposed adjacent only one side of the gate.

63. (New) The method of claim 22 wherein the drain region is disposed adjacent only one side of the gate.

64. (New) The method of claim 22 wherein the source region and drain region are disposed directly opposite one another on opposite sides of the gate.

65. (New) A method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle;

filling the first and second isolation trench portions with dielectric material;

wherein forming the first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

66. (New) The method of claim 65, wherein etching and depositing comprises:

providing a mixture of gasses chosen from a group consisting of CF_4, CHF_3, CH_2F_2 and C_2F_8; and

supplying radio frequency excitation to the mixture.

67. (New) The method of claim 65, wherein etching and depositing comprises:

providing fluorocarbon gases; and

supplying radio frequency excitation to the mixture.

68. (New) A method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material;

wherein forming the first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67;

depositing a polymer on the sidewalls during plasma etching;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing depositing polymer on the sidewalls; and

stopping etching and depositing when the predetermined interval ends.